Call for Proposals

Engineering Technology

HIRP OPEN 2017

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Application Deadline: 09:00 A.M., 16th June, 2017 (Beijing Standard Time, GMT+8).

If you have any questions or suggestions about HIRP OPEN 2017, please send Email (innovation@huawei.com). We will reply as soon as possible.

Catalog

HIRPO2017080401: Design Wireless Charging Prototype for Consumer Electronics

1 Theme: Engineering Technology

2 Subject: Based on resonance principle for middle range wireless power transfer applications

List of Abbreviations

WPT	Wireless Power Transfer

3 Background

The endurance of battery within intelligent terminal equipments has been plaguing people. Wireless charging technology because of its convenience, there seems to be an opportunity to improve this situation. In particular, resonance wireless charging technology, can achieve a relatively long distance charging of consumer electronics.

So, it is valuable to research middle range wireless power transfer applications base on resonance wireless charging technology.

4 Scope

Design a wireless power supply system, the performance indicators are as follows：

Input and output specifications: input DC voltage 5V, output DC voltage 5V, output power can reach to 0.3w;

The maximum geometry of the transmitter is not more than 70mm*70mm*70mm (including the transmitter coil and power circuit);

Receiving coil volume not exceeding 2cm^3 ; the receiving side power circuit does not exceed than 20mm*20mm*2mm;

When the receiver output power reach to 0.3w, the wireless power supply system conversion efficiency should be reach to 15% (the nearest distance from transmitter to receiver is greater than or equal to 10cm, the efficiency test including TX power circuit and Rx power circuit and both side coils.);

5 Expected Outcome and Deliverables

Technical reports of WPT model and analysis for middle range wireless power supply system;

Technical reports of WPT solution design, including theoretical optimal system parameters analysis, the performance simulation of the scheme;

Wireless power supply system prototype;

1~2 Invention/patents;

6 Acceptance Criteria

1) Project proposal is accepted by the evaluation team, Huawei.
2) Project deliverables are accepted by the evaluation team, Huawei.
3) The prototype performance indicators meet the requirements.

7 Phased Project Plan

Phase1 (~3 months): survey the state of middle range wireless power transfer field, analyze and build the WPT model and provide the related technical report.

Phase2 (~6 months): Design wireless power transfer prototype and provide the related technical report、simulation model and results.

Phase3 (~3 months): WPT system optimization and provide patents.

Click here to back to the Top Page

HIRPO2017080402: Improvement on EMI reduction for spatial noise

1 Theme: Engineering Technology

2 Subject: EMI reduction for spatial noise

List of Abbreviations

EMI	electromagnetic interference
PCB	Printed Circuit Board

3 Background

Electromagnetic interference (EMI) is a disturbance that affects an electrical circuit due to electromagnetic conduction or electromagnetic radiation emitted from an external source. EMI reduction is a serious problem in modern electronics and communication systems. One of the weakest points is the amount of electromagnetic noise energy would radiate from an interference source to nearby antenna or receiver circuits. Enclosures made of metal alloys have often been used for this problem. But external problems would be created: 1) Electromagnetic noise can escape from slots between enclosures and PCB as shown in figure 1. Currently, screws and conductive adhesive are used for that purpose. But screws may cause stress problems and conductive adhesive would become invalid from the intense heat. 2) As the frequency rise up to 25GHz, cavity resonance is unavoidable only by downsizing the cavity. The general use of microwave absorbing materials has cost problems. A low cost method is to be exploited.

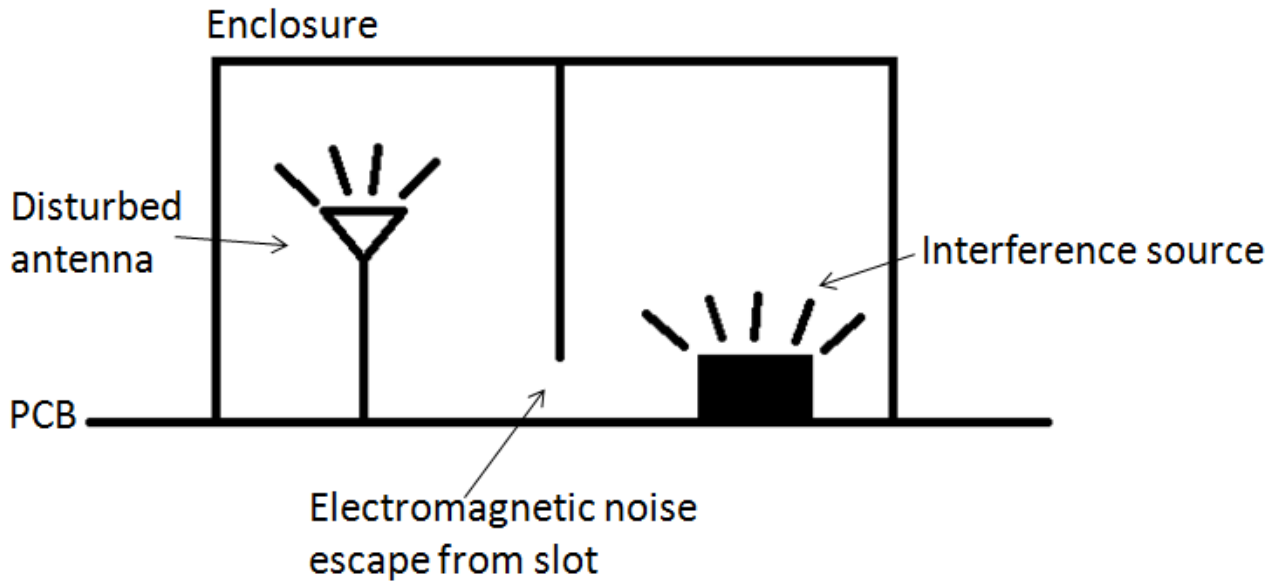

Figure 1. EMI problem caused by slots between enclosures and PCB

4 Scope

Research on methods for EMI suppression: A strategic goal of the project is to develop a technology for spatial noise suppression when enclosures are used on PCB. There are two problems: 1) How to suppress the noise from slots without using screws and conductive adhesive; 2) How to solve cavity resonant problem by a low cost way. Some structures (may be EBG structures) or methods would be used in a finite space for wideband EMI reduction.

5 Expected Outcome and Deliverables

We are expecting to get below deliverables through this project:

For problem 1: The working frequency should cover from 700MHz to 6GHz; The isolation between antennas should improve over -20dB.

For problem 2: At frequencies above 25GHz, a low cost method for cavity resonant suppressing is expected to replace currently used microwave absorbing materials.

6 Acceptance Criteria

at least one patent.

The isolation between micro-stripe lines over 20dB improved in a band frequency from 700MHz to 6GHz for problem 1.

The result of suppressing method should be comparable with microwave absorbing materials for problem 2.

Low cost method.

7 Phased Project Plan

Phase1 (~3 months): survey the state of spatial noise suppressing method, provide basic method and simulation results.

Phase2 (~6 months): Design spatial noise suppressing method and provide the related technical report、simulation model and results.

Phase3 (~3 months): method optimization and provide patents.

Click here to back to the Top Page

HIRPO2017080701: The Exploration of Auto–Code-Generation Technologies and Potential Applications

1 Theme: Engineering Technology

2 Subject: Artificial Intelligence, Engineering Technology, Big Data

List of Abbreviations

NA

3 Background

To accomplish many common coding tasks, huge amount of functionalities provided by numerous libraries and frameworks have been increasingly relied by programmers.

One traditional example is that: software developers today have made heavy use of the code completion support found in modern source code editors. Most editors provide code completion in the form of a floating menu containing contextually-relevant variables, fields, methods, types and other code snippets. Several refinements and additions to the code completion menu have previously been suggested in the literature. Some have focused on leveraging additional sources of information, such as databases for usage history， inheritance information, API-specific information, partial abbreviations, examples extracted from code repositories and crowd sourced information, to increase the relevance and sophistication of the featured menu items.

Nowadays, we have Big Code Data which enable us to obtain large amount of codes, related documents, related bug lists and related application backgrounds. Our interests include how to use a large number of history codes obtained from Github and other repositories, also with Huawei's own code repositories to generate a code section or method completion during coding process, or maybe finding similar possible bugs according to the project area and histories. Furthermore, by auto-fixing similar bugs based on the debugging histories is also what we are interested in.

4 Scope

1). Based on code repositories such as code obtained from Github, documents or other related information, the idea and realization method on how to use the big code data to realize an auto-code-generation demo.

2).The auto-code-generation program would include code-completion, code/API recommendation, auto-bug-fixer, similar-bug-auto-fixer or any similar products. The technology should consider using program context such as information from other special projects, coders, departments, functions and other applications related to auto-generation.

3). Technologies such as machine learning, deep learning, NLP, static analysis etc. are acceptable. Applications of machine learning/ deep learning using historic repository data is much preferred.

5 Expected Outcome and Deliverables

1). Technical reports on auto-code-generation technologies and future development direction;

2). A prototype tool should be delivered, including training dataset, testing dataset, the tool, source code, and related documents.

6 Acceptance Criteria

Project proposal will be evaluated and approved by the evaluation team, Huawei.

Project deliverables will be evaluated and approved by the evaluation team, Huawei.

7 Phased Project Plan

Phase1 (~3 months): survey the state of art of auto-code generation technology, analyze the business scenarios, make overall technical solutions, and provide related technical report.

Phase2 (~7 months): design and implement the algorithms for code-completion, code/API recommendation, auto-bug-fixer, similar-bug-auto-fixer or other similar products. Provide the related prototype tool, source code, and design documents.

Phase3 (~2 months): evaluation and optimization of the tool. Optimize the algorithm and implementation to improve the reliability, accuracy, and efficiency of the algorithm.

Click here to back to the Top Page

HIRPO2017080901: Real-time DNN-based Motion Blur Removing for Mobile Cameras

1 Theme: Engineering Technology

2 Subject: Terminal electromagnetic simulation

List of Abbreviations

DNN	Deep Neural Network
SLR Camera	Single-lens Reflex Camera

3 Background

Mobile handset camera is among the most important and most frequently used features to our consumers. A good photography feature will play a key factor in customers' mobile devices purchase decisions. Explanations for this are many, for instance:

- People today share their daily lives frequently on social media using mobile devices.
- Sometimes a retake is difficult if one shooting does not come out satisfying.
- More and more photography enthusiasts rather use mobile cameras than professional cameras such as SLR cameras to shoot because of its convenience.

However, comparing to professional cameras such as SLR cameras, photos shooting by mobile handset cameras suffer even more from image degradation. One major source of image degradation is image blur, and deblurring has been a popular research topic in the field of image processing

since 1960s. Although a deal of research has been devoted into this field, there are still some challenges to be overcome.

Various reasons can cause image blur, examples are:

- the atmospheric turbulence --- Gaussian Blur,
- camera relative motion during exposure --- Motion Blur,
- lens aberrations --- Defocus Blur,
- Combinations of multiple blur causes --- Non-uniform Blur.

A typical blurred image Y can be represented as

$$Y = K * X + N,$$

eq. (1)

where X denotes the sharp image, N refers to additive noise, and K denotes a blur kernel.

Most traditional Deblur methods try to guess the kernel K and noise N to recover sharp images from blurry images. However, limiting by large computational resource demand, and ill-posed nature of the problem, traditional Deblur methods are far from implementing real time Deblur on mobile devices while achieving state-of-art performance.

Until recently, an innovative Deblur approach are introduced, which try to solve Deblur problem by using DNN. Instead of “guessing” blur kernels by researcher, DNNs are trained by a large amount of blurred images and sharp images to adjust “parameters” in the “neurons”. This method can also achieve state-of-art performance, while keeping the calculation time down. Therefore, this project is intended to encourage research and design real time solutions to remove image motion blur by DNN for mobile devices.

4 Scope

Investigate variety kinds of image blur on mobile cameras, research on removing motion blur from images in a timely fashion.

Design solutions, based on DNN, to quickly remove motion blur on the image.

We summarized several motion blur types as follows, the camera shake blur should be concerned as first priority:

- Camera shake (motion blur caused by shooters at exposure)
- Object movement (motion blur caused by moving object)
- Non-uniform motion blur (combination blur, spatially-varying blur, or pixels blurred differently)

5 Expected Outcome and Deliverables

- A state-of-art deblur solution for mobile devices to remove motion blur at real-time using DNN
- Training & testing set of the network
- DNN models
- A state-of-art technical report of motion blur removing models for mobile cameras
- 1~2 Invention/patents

6 Acceptance Criteria

- Project proposal is accepted by the evaluation team, Huawei.
- Project deliverables are accepted by the evaluation team, Huawei.
- The proposed solution can improve quality of images at human eye level in

a competitively short period of time.

7 Phased Project Plan

Phase1 (~3 months): survey the state of the art of motion blur removing algorithms in industrial and academic image processing field, identify the problems, metrics and build the draft model for motion blur removing, provide the related technical report.

Phase2 (~5 months): complete motion blur removing model that can reach state-of-art performance with relative short execution time, provide the model design and evaluation report.

Phase3 (~4 months): improve motion blur removing model to meet the acceptance criteria, compress and fine-tune the model, and provide the final model and evaluation report.

Click here to back to the Top Page

HIRPO2017080902: The simulation of digital chip ESD protection

1 Theme: Engineering Technology

2 Subject: Terminal electromagnetic simulation

List of Abbreviations

ESD	Electro Static Discharge
CMOS	Complementary Metal Oxide Semiconductor
LDD	Lightly Doped Drain
I/O	Input and Output

3 Background

The damage of CMOS IC caused by electrostatic discharge is a well-known reliability problem. When the CMOS process is reduced to micron scale, advanced process technology, such as thinner gate oxide layer, a shorter channel length, the more shallow source depth, LDD, and metal silicide diffusion layer, these advanced process seriously reduce the electrostatic protection ability of CMOS IC. Therefore, the micron CMOS IC urgently needs an effective and reliable ESD protection simulation design to predict.

There are all kinds of input and output ESD protection design with hundreds of patents. However, in the practical application and simulation, it is not widely to control, we could not predict the chip's ESD protection ability by

simulation. Also, the internal CMOS IC suffered abnormal damage could not be predicted by simulation by now.

So, it's valuable to develop a set of ESD simulation solution for I/O and whole chip to improve IC ESD protection ability, and ultimately improve the ESD protection ability of terminal device.

4 Scope

Investigate chip protection circuit design institutes and companies

Investigate institutions and companies which are deep into chip FA analysis

Investigate institutions and companies which are deep into ESD testing and simulation

5 Expected Outcome and Deliverables

- The mechanism of digital chip damage.
- Current digital chip test specification.
- Modeling of digital port.
- ESD Simulation methodology of digital port.
- The error of voltage or current between simulation and measurement is less than 20%.

6 Acceptance Criteria

To create a simulation methodology of digital chip ESD protection, which is corresponding with test specification and modeling, to improve the ESD protection of digital chip.

7 Phased Project Plan

Phase1 (~1 months): The mechanism of digital chip damage.

Phase2 (~1 months): Current digital chip test specification.

Phase3 (~4 months): Modeling of digital port.

Phase4 (~4 months): ESD Simulation methodology of digital port.

Click here to back to the Top Page

HIRPO2017080903: The simulation of analog chip ESD protection

1 Theme: Engineering Technology

2 Subject: Terminal electromagnetic simulation

List of Abbreviations

ESD	Electro Static Discharge
CMOS	Complementary Metal Oxide Semiconductor
LDD	Lightly Doped Drain
I/O	Input and Output
PA	Power Amplifier

3 Background

The damage of CMOS IC caused by electrostatic discharge is a well-known reliability problem. When the CMOS process is reduced to micron scale, advanced process technology, such as thinner gate oxide layer, a shorter channel length, the more shallow source depth, LDD, and metal silicide diffusion layer, these advanced process seriously reduce the electrostatic protection ability of CMOS IC. Therefore, the micron CMOS IC urgently needs an effective and reliable ESD protection simulation design to predict.

There are all kinds of input and output ESD protection design with hundreds of patents. However, in the practical application and simulation, it is not widely to control, we could not predict the chip's ESD protection ability by simulation. Also, the internal CMOS IC suffered abnormal damage could not be predicted by simulation by now.

So, it’s valuable to develop a set of ESD simulation solution for I/O and whole chip to improve IC ESD protection ability, and ultimately improve the ESD protection ability of terminal device.

4 Scope

Investigate chip protection circuit design institutes and companies;

Investigate institutions and companies which are deep into chip FA analysis;

Investigate institutions and companies which are deep into ESD testing and simulation methodology.

5 Expected Outcome and Deliverables

- The mechanism of analog chip damage;
- Current analog chip test specification;
- Modeling of analog port;
- ESD Simulation methodology of analog port;
- The error of voltage or current between simulation and measurement is less than 20%.

6 Acceptance Criteria

To create a simulation methodology of analog chip ESD protection, which is corresponding with test specification and modeling, to improve the ESD protection of analog chip.

7 Phased Project Plan

Phase1 (~1 months): The mechanism of analog chip damage.

Phase2 (~1 months): Current analog chip test specification.

Phase3 (~4 months): Modeling of analog port.

Phase4 (~4 months): ESD Simulation methodology of analog port

Click here to back to the Top Page

HIRPO2017080904: The research of TP/LCD modeling for simulation

1 Theme: Engineering Technology

2 Subject: Terminal electromagnetic simulation

List of Abbreviations

ESD	Electro Static Discharge
TP	Touch Panel
LCD	Liquid Crystal Display

3 Background

The ESD problems of TP/LCD can be divided into two kinds, software and hardware damage.

“Ghost hand (the wrong operation)”, abnormal display etc. are belong to software damage. IC damage, TFT array damage etc. are belong to hardware damage.

During the mobile phone development process, TP/LCD ESD problems produced more than 60% of all ESD problems, and there is still no effective methodology to solve the problem, could rely on the supplier of TP/LCD solution. However, the period of development is hardly to guarantee, therefore, it’s valuable to establish a methodology of simulation and testing ability, strictly control the performance of ESD TP/LCD to ensure the period of development.

4 Scope

1) Investigate institutions and companies which are deep into TP/LCD FA analysis;
2) Investigate institutions and companies which are deep into ESD testing and simulation.

5 Expected Outcome and Deliverables

The mechanism of TP/LCD damage;

Current TP/LCD test specification;

Develop the TP/LCD testing specification and system base on mobile device (including module and whole device);

Develop a methodology of TP/LCD ESD simulation according to the testing;

The error of voltage or current between simulation and measurement is less than 20%.

6 Acceptance Criteria

Develop a methodology of TP/LCD modeling and ESD simulation according to test specification to improve the ESD robustness of TP/LCD, reduce the TP/LCD ESD problem to less than 20% of all ESD problems.

7 Phased Project Plan

Phase1 (~1 months): Failure analysis of TP/LCD damage;
Phase2 (~1 months): Investigate current TP/LCD test specification;
Phase3 (~4 months): Develop the TP/LCD testing specification base on mobile device (including module and whole device);

Phase4 (~4 months): Develop a methodology of TP/LCD ESD simulation according to the testing

Click here to back to the Top Page

HIRPO2017080905: RCV and SPK accurate simulations

1 Theme: Engineering Technology

2 Subject: Terminal electromagnetic simulation

List of Abbreviations

RCV	Voice Receiver
SPK	Sound Speaker
EM	Electromagnet

3 Background

As the audio demanding developing, the users of cellphones need higher level quality of sounds and music. In the phone, the audio system is approximately divided into 3 part in physical the codec, the connections with filters and the audio device. The audio devices are responsible for converting the electric signals into sound signals, which turn voltage and current into mechanical vibration. This procedure may include many kind of fields in different physical domain. Thus how to simulate and emulate these devices by combining multi-physics is a challenge for us. We propose this project to find a co-operator to help us setup simulation flows, and finally we could optimize the design using simulation.

4 Scope

EM to mechanical simulation with non-linear effect include

If we give the exact model of an audio device then we can setup the EM and sound relations of the device by simulations and validation are accurate enough.

5 Expected Outcome and Deliverables

- Technical reports of EM to sound simulation theory;
- Workflow reports of audio device simulation;
- Validation results
- 1~2 Invention/patents;

6 Acceptance Criteria

The simulated results could compare with the measurement results within 5% error;

7 Phased Project Plan

Phase1 (~3 months): survey the multi-physical simulation method and provide the related technical report.

Phase2 (~6 months): research the workflow and measure the test results and provide the related technical report.

Phase3 (~3 months): research and provide related algorithms, simulation results and patents.

Click here to back to the Top Page